**In the Drawings**

Please delete sheet 1 and insert the attached Replacement Sheet containing FIGS. 1 and 2.

## REMARKS

Claims 1-10 and 21-28 are pending in the application with the present amendments. Claims 11-20 which were not elected in response to the restriction requirement, are cancelled herein. With the attached Replacement Sheet, FIGS. 1 and 2 are amended herein to incorporate the legend "PRIOR ART" as required by the Examiner. The title is amended herein to refer only to a bipolar transistor as now claimed herein, as well as to correct a prior transcription error of the term "collector-base" capacitance. No new matter is incorporated by the present change to the drawings or the title.

The Applicants appreciate the indication of allowability provided by the Examiner as to claim 2. Claim 2 is amended herein to incorporate the recitations of claim 1 from which it formerly depended, making it immediately allowable. New claims 21 through 28, which depend from claim 2 and which include recitations similar to those of claims 3 through 10, are submitted to be allowable at least on the same basis as claim 2.

In the Office Action, claim 1 and claims 3 through 10 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,798,561 to Sato ("*Sato*"). For the reasons set forth below, applicants submit that amended claims 1 and 3 through 10 which depend from claim 1 are fully distinguished from *Sato*.

In paragraph 8 of the Office Action, the Examiner equates the bipolar transistor claimed in claim 1 with bipolar transistors shown in FIGS. 3, 5 and 10 of *Sato*. An essential feature of claim 1 is a dielectric region disposed in an undercut *directly underlying* the intrinsic base region. (See dielectric region 54 shown in FIG. 3 of the present

application which directly underlies the intrinsic base layer 112).

With respect to unamended claim 1, the Office Action indicated that the dielectric regions 4, 6 (FIG. 3) of *Sato* are disposed in an undercut underlying the intrinsic base layer 12a. With respect to the *amended* claim 1, it is abundantly clear from the marked up drawings of *Sato* appended below, that *Sato* neither teaches nor suggests a "dielectric region disposed in an undercut *directly underlying* the intrinsic base layer." In each case, the dielectric regions shown in *Sato* do not directly underlie the intrinsic base layer, but rather, are laterally spaced therefrom. See attached marked FIGS. 3, 5 and 10 of *Sato*.

FIG.3

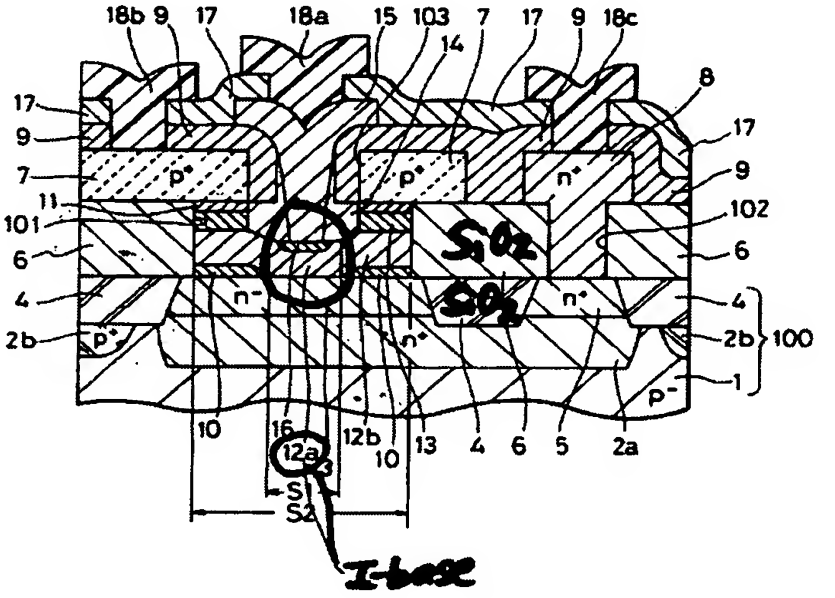


FIG.5

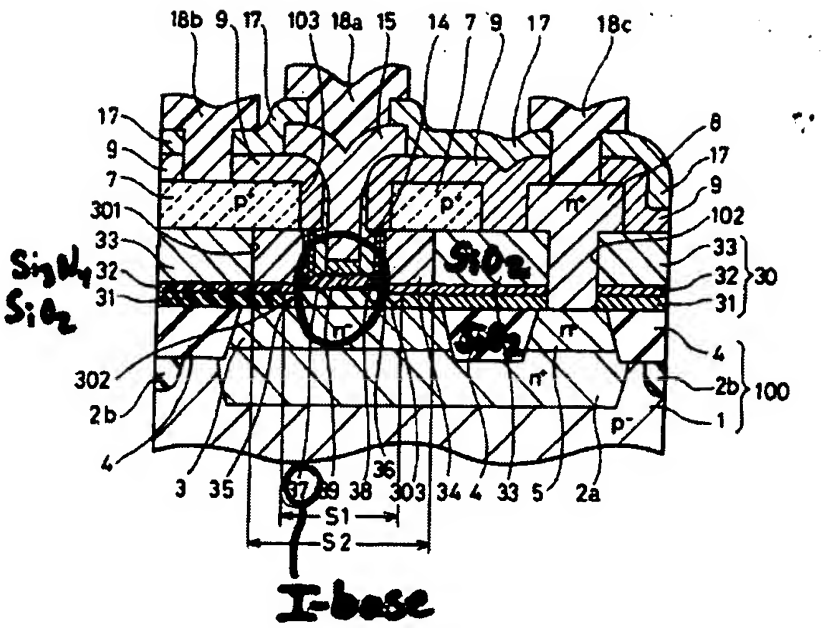
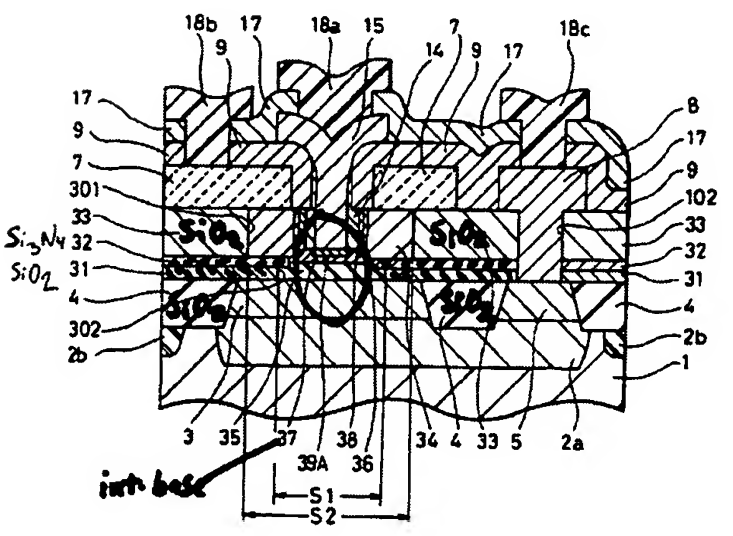



FIG.10




For the foregoing reasons, applicants submit that the application is in immediate condition for allowance. The Examiner is requested to contact the undersigned by telephone if there is any question regarding the present submission which can be resolved in order to pass the application to allowance.

This Amendment is filed together with a petition for extension of time (one month). It is believed that no other fees are required to be filed in connection with this Amendment. However, if any fees are required, authorization is given to debit the Deposit Account No. 09-0458 of the Assignee International Business Machines Corporation. If there is an overpayment, please credit the same account.

Respectfully submitted,
**Hiroyuki Akatsu et al.**

By: _____

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